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ABSTRACT

The present invention provides integrated circuit fabrication methods and devices wherein dual damascene structures (552 and 558) are formed in a dielectric stack including three dielectric layers (516, 518 and 530). Via patterns (522 and 524) for these structures have a rectangular shape and are wider than the corresponding overlaying trench patterns (534 and 536). Another embodiment of the present invention provides dual damascene structures (860 and 862) employing a sacrificial etch segment (828) in an etch stop layer (818) of a dielectric stack (810, 816 and 842). The sacrificial etch segment is positioned between adjacent dual damascene interconnect lines (864 and 866) which are formed on the etch stop layer (818). In additional embodiments, manufacturing systems (1210) are provided for fabricating IC structures. These systems include a controller (1200) which is adapted for interacting with a plurality of fabrication stations (1220, 1222, 1224, 1226, 1228 and 1230).